REMARKS

Applicants are including a petition to amend the drawings in the same package as the present Response, wherein Figure 1 is amended to include the legend, "Prior Art". As a result, the objection to Figure 1 is overcome.

Claims 1-7, 9-13, 16-17, 19-20 and 22-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) and Hariguchi (U.S. Patent 6,307,855).

Claim 1 recites "a plurality of content addressable memory (CAM) blocks, each configured to provide a hit signal and an index signal in response to an applied address".

The Examiner indicates that Figure 6 of Hariguchi teaches that each CAM block is configured to provide a hit signal (on entry hit line 72) and an index signal (on mask value lines 86) in response to an applied address.

Contrary to the Examiner's assertion, Hariguchi does not teach "an index signal" as recited by Claim 1. Hariguchi teaches that mask index register 80 stores a prefix length associated with the destination IP address stored in the CAM block. (Hariguchi, Col. 9, lines 3-6.) The mask index register 80 provides this prefix length on mask value lines 86. (Hariguchi, Col. 7, lines 40-41.) Thus, Hariguchi teaches that each 'CAM block' provides a signal that identifies the prefix length of a stored address, and not an index value.

It is important to note that each 'CAM block' described by Hariguchi only stores a single destination address (i.e., a single entry). For this reason, Hariguchi has no need for 'an index signal', which would identify the location of a hit within the CAM block.

Moreover, Hariguchi teaches that the mask index register 80 outputs the prefix length on the mask value lines 86 regardless of the state of an applied address. (Hariguchi, Col. 7, lines 40-41.) Thus, Hariguchi fails to teach that the CAM block provides "an index signal in response to an applied address" as recited by Claim 1.

For these reasons, AAPA and Hariguchi fail to teach "a plurality of content addressable memory (CAM) blocks, each configured to provide a hit signal and an index signal in response to an applied address" as recited by Claim 1.

In addition, Claim 1 recites "a plurality of programmable storage elements configured to store a plurality of routing values" and "a configurable switching circuit coupled to receive the hit signals from the CAM blocks and the routing values from the programmable storage elements, wherein the configurable switching circuit routes the hit signals in a first order in response to the routing values".

The Examiner indicates that the 'programmable storage elements' and 'configurable switching circuit' are taught by the routing engine 400 of Figure 8 of Hariguchi, which includes routing table 320, ARP table 322 and routing result generator 324.

Hariguchi teaches that the routing table 320 of Figure 8 is implemented using one of the CAM blocks of Figs. 1-7. (Hariguchi, Col. 3, lines 60-61.) However, the Examiner does not indicate how these CAM blocks teach 'programmable storage elements' or 'a configurable switching circuit' as recited by Claim 1. Moreover, Hariguchi does not provide any details concerning the circuitry implemented by the ARP table 322 or the routing result generator 324 of the routing engine 400. The routing engine 400 of Hariguchi

therefore does not teach "programmable storage elements" or "a configurable switching circuit" as recited by Claim 1.

Claim 1 further recites "a first multiplexer configured to route one of the routing values from the programmable storage elements as an index routing value in response to the output hit signal" and "a second multiplexer configured to route an index signal from one of the CAM blocks as an output index value in response to the index routing value".

The Examiner indicates that these multiplexers are shown by the circuitry in Figures 7 and 8 of Hariguchi. However, the Examiner does not indicate which elements of Figures 7 and 8 of Hariguchi correspond with 'a first multiplexer' and 'a second multiplexer' as recited by Claim 1. If the Examiner believes that Figures 7 and 8 of Hariguchi teach 'a first multiplexer' and 'a second multiplexer' as recited by Claim 1, he is required to indicate where these figures provide such a teaching.

For these reasons, Claim 1 is allowable over AAPA in view of Hariguchi. Claims 2-7 and 9-13, which depend from Claim 1, are allowable over AAPA in view of Hariguchi for at least the same reasons as Claim 1.

In addition, Claim 2 recites 'wherein the index routing value and the output index value are provided to access the SRAM array'. Contrary to the Examiner's assertion, AAPA does not teach that both an output index value and an index routing value are provided to access the SRAM array 240. Rather, AAPA teaches that only an output index value is provided to the SRAM array. For this additional reason, Claim 2 is allowable over AAPA in view of Hariguchi.

In addition, Claim 4 recites 'the configurable switching circuit comprises a plurality of multiplexers, each corresponding with one of the CAM blocks, and each being coupled to receive all of the hit signals from the CAM blocks'. The Examiner indicates that comparator 210 in Fig. 5 of Hariguchi corresponds with the multiplexers recited in Claim 4. It is first noted that a comparator is not a multiplexer. In addition, comparator 210 is part of CAM cell 220, an therefore cannot constitute a multiplexer in a configurable switching circuit external to the CAM block. Moreover, comparator 210 is not 'coupled to receive all of the hit signals from the CAM blocks' as recited by Claim 4. For these additional reasons, Claim 4 is allowable over AAPA in view of Hariguchi.

In addition, Claim 9 recites "the asserted hit signal having the highest priority and the output index value originate in the same CAM block". In contrast, Hariguchi teaches that the asserted hit signals (provided on entry hit lines 72) originate in CAM entries 230, but the output index value (e.g., the hit entry address, is provided by prioritizer 100 on hit entry bus 102. (Hariguchi, Col. 8, lines 1-3.) For this additional reason, Claim 9 is allowable over AAPA in view of Hariguchi.

Claim 16 recites 'generating a hit signal and an index signal with each of the CAM blocks in the first and second sets of CAM blocks in response to the input address'. As described above in connection with Claim 1, AAPA and Hariguchi fail to teach generating an "index signal" with each of the CAM blocks. As also described above in connection with Claim 1, AAPA and Hariguchi fail to teach that the CAM block provides "an index signal … in response to … [an] input address" as recited by Claim 16.

In addition, Claim 16 recites 'storing a plurality of routing values in a programmable register' and 'routing the hit signal generated by each of the CAM blocks to a priority encoder in an order determined by the routing values'. In contrast, AAPA teaches that the prefixes must be stored in CAM array 202 in an order arranged from highest priority to lowest priority. (Specification, Paragraph [0008].) Consequently, hit signals are provided from CAM array 202 to priority encoder 230 in this same order. Thus, AAPA fails to teach "routing hit signals generated by each of the CAM blocks to a priority encoder in an order determined by the routing values" as recited by Claim 16.

Moreover, Claim 16 recites "routing one of the routing values as an index routing value in response to the output hit signal" and "routing one of the index signals as an output index value in response to the index routing value". The Examiner indicates that the routing engine 400 illustrated by Fig. 8 of Hariguchi teaches these steps. However, even if Hariguchi teaches that routing engine 400 sends the routing result back to the header translator to determine the port used (as indicated by the Examiner), this does not mean that the routing engine 400 implements the above-cited routing steps as recited by Claim 16.

For these reasons, Claim 16 is allowable over AAPA and Hariguchi. Claims 17, 19-20 and 22-23, which depend from Claim 16, are allowable over AAPA and Hariguchi for at least the same reasons as Claim 16.

In addition, Claim 17, which recites 'using the index routing value and the output index value to address a memory array', is further allowable over AAPA and

Hariguichi for reasons similar to Claim 2 (described above).

In addition, Claim 20, which recites 'the asserted hit signal having the highest priority and the output index value originate in the same CAM block', is further allowable over AAPA and Hariguchi for reasons similar to Claim 9 (described above).

Claims 8 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hariguchi, and Pereira et al. (U.S. Patent 6,249,467).

Claim 8, which depends from Claim 1, is allowable over AAPA and Hariguchi for at least the same reasons as Claim 1. Pereira et al. do not remedy the above described deficiencies of AAPA and Hariguchi. Consequently, Claim 8 is allowable over AAPA, Hariguchi and Pereira et al.

Claim 21, which depends from Claim 16, is allowable over AAPA and Hariguchi for at least the same reasons as Claim 16. Pereira et al. do not remedy the above described deficiencies of AAPA and Hariguchi. Consequently, Claim 21 is allowable over AAPA, Hariguchi and Pereira et al.

Claims 8 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hariguchi, and Nusinov et al. (U.S. Patent 5,467,319).

Claim 8, which depends from Claim 1, is allowable over AAPA and Hariguchi for at least the same reasons as Claim 1. Nusinov et al. do not remedy the above described deficiencies of AAPA and Hariguchi. Consequently, Claim 8 is allowable over AAPA, Hariguchi and Nusinov et al.

Claim 21, which depends from Claim 16, is allowable over AAPA and Hariguchi for at least the same reasons as Claim 16. Nusinov et al. do not remedy the above described

deficiencies of AAPA and Hariguchi. Consequently, Claim 21 is allowable over AAPA, Hariguchi and Nusinov et al.

Applicant notes the allowability of Claim 24. Applicant further notes that Claim 18 was not rejected, and should therefore be indicated as being allowable.

Claims 14 and 15 have been objected to as being dependent upon a rejected base claim. The Examiner has indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Because Applicant believes that the base claim is allowable for reasons stated above, Applicant is not amending Claims 14 and 15 at this time.

CONCLUSION

Claims 1-24 are pending in the present application. Claims 18 and 24 are allowed, and Claims 14 and 15 are allowable. Reconsideration and allowance of Claims 1-13, 16-17 and 19-23 is requested. If the Examiner has any questions, he is invited to call the undersigned at (925) 895-3545.

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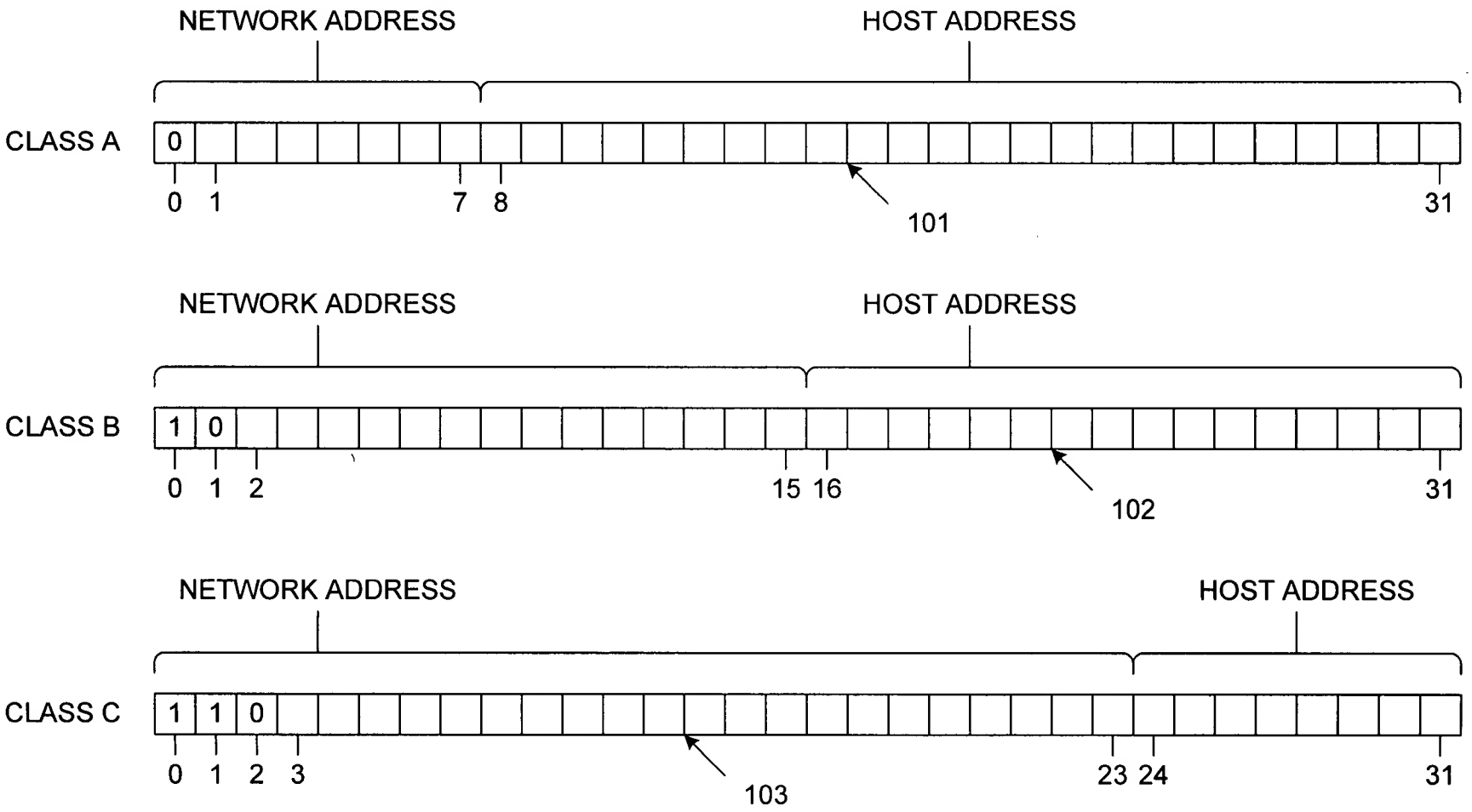

FIG. 1

(PRIOR ART)